Ultrahigh Resolution Frequency Measurement Scheme Based on Phase Relationship between Period Groups

Faxi Chen[1], Wei Zhou[1],Zi Ye[2], Hai Wang[1]
[1]Dept. of Measurement and Instrument, Xidian University, Xi'an, 710071, P. R. China
[2]Dept. of Information Science and Engineering, Zhejiang University, Hangzhou, 310058, P. R. China

***Abstract*—To achieve high resolution in frequency measurement, an depth analyzing of the group phase relationship between two signals with different frequencies is done, on which an ultrahigh resolution measurement scheme by detecting the optimal group phase coincidence is presented. The method is implemented on a CPLD chip, and the actual measurement data of the prototype shows that its resolution is approximately $10^{-13}/\tau$ order of magnitude. This scheme is simple in circuit, high in measurement resolution, and low in cost. So it shows a wide promotion and application value.**

I. INTRODUCTION

With the development of high-tech, such as aviation, aerospace and communication, the higher resolution in frequency measurement is needed. However the instrument which can achieve higher resolution in frequency measurement is of complex structure, high cost and large volume. An ultrahigh resolution frequency measurement scheme is proposed in this paper, which is implemented with simple structure and low cost in small volume.

II. FREQUENCY MEASUREMENT SCHEME BASED ON PHASE RELATIONSHIP BETWEEN PERIOD GROUPS AND ITS ERRORS

There is a periodic regularity between the phases of two signals with frequency difference [1]. If frequencies of two signals are $f_0=Af_{maxc}$ and $f_x=Bf_{maxc}$ respectively, where the two positive integers A and B are prime with each other, $f_{maxc}$is the maximum common factor frequency between f_0 and f_x. When the group phase coincidence occurs [2], the time interval between two group phase coincidences $T_{minc}=1/f_{maxc}$, is called minimum common multiple period. Using the time of integer multiples T_{minc} as counter gate, the counter gate would be synchronized with f_0 and f_x, therefore the ±1 count errors will be eliminated[3]. And then, with the equation(1), the value of f_x can be obtained.

$$f_x = f_0 * N_x / N_0 \quad (1)$$

Obviously, if the counter gate begin at the moment of the group phase coincidence, and end after several T_{minc}'s, the resolution in frequency measurement would be improved greatly. So the key to this method is how to detect the optimal group phase coincidence.

In actual conditions, the maximum common factor frequency, f_{maxc} , between f_0 and f_x is quite small. For example, if f_0=5000001Hz and f_x = 4000000Hz, that is f_{maxc} = 1Hz, T_{minc}=1s. Observed in a short time, their phase variation regularity is quite similar to the condition in which f_0=5000000Hz and f_x = 4000000Hz,. In order to be analyzed conveniently, take A'=5, B'=4, f'_{maxc} = 1000000Hz and T'_{minc} = 1μs as approximation. Theoretically, there is only one group phase coincidence in every T_{minc}. However, the least quantization phase shift resolution of f_0 and f_x ,

$$\Delta T = 1/AB\, f_{maxc} \quad (2)$$

is about 0.05ps, which is out of any component's resolution. So, whatever method used, the group phase coincidence detected is not single but a group. Near the accurate group phase coincidence, there are thousands of approximate group phase coincidence.

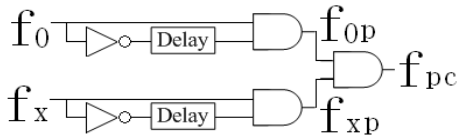

Figure 1. Circuit of group phase coincidence detection

A highly-efficient group phase coincidence detection circuit is showed in Fig.1, and its waveform is showed in Fig. 2.

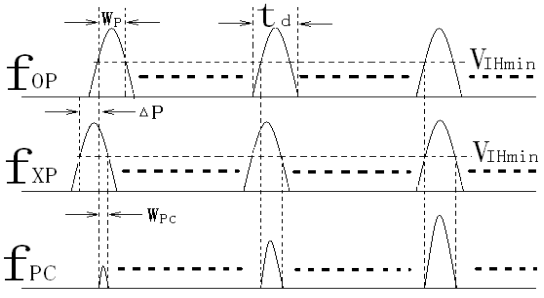

Figure 2. Waveform Of group phase coincidence detection circuit

This Paper is Supported by the National Science Foundation of China under Grant NO. 60772135 and NO.10703004

Where f_{op} and f_{xp} are the narrow pulses created by the rising edges of f_{op} and f_{xp} respectively, t_d is the pulse width of f_{op} and f_{xp}, and W_p is the width of the pulse part of which the voltage is higher than minimum high-level input voltage,V_{IHmin}. Usually $V_{IHmin}=V_{CC}/2$ in COMS technology, there is

$$W_p = t_d - t_r \quad (3)$$

where t_r is the rising time of f_{op} and f_{xp}. Sending f_{op} and f_{xp} to an And Gate, the phase coincidence pulse f_{pc} can be gotten, whose width is W_{pc}. When $|\Delta P| < W_p$, whereΔP is the phase difference of f_0 and f_x that is

$$W_{pc} = W_p - |\Delta P| \quad (4)$$

And if $|\Delta P| > W_p$, there will be

$$W_{pc} = 0 \quad (5)$$

During the process that the phase relationship between f_0 and f_x from group phase coincidence to next group phase coincidence, the W_{pc} trends to change from wide to narrow, and then from narrow to wide. It should be noticed that if the relationship of A' and B' is complex, the width of adjacent f_{pc} is not simply monotonic. Supposing that the number of phase coincidence pulses f_{pc} is N, if $t_d > t_r$, that is

$$N = W_p/\Delta T = (t_d - t_r)/\Delta T \quad (6)$$

And when $t_d < t_r$, there will be

$$N = 0 \quad (7)$$

Among these N phase coincidence pulses, there is a accurate phase coincidence pulse, of which $|\Delta P| = 0$. On an ideal condition, the accurate phase coincidence pulse can be detected, but it is hardly in fact. So it is necessary to detect an optimal group phase coincidence pulse among these approximate group phase coincidence pulses.

To trigger the control circuit of the counter gate, the triggering voltage must be higher than V_{IHmin} , it is said that only when $W_{pc} > t_r$ the control circuit can work. Among N phase coincidence pulses, let the number of phase coincidence pulses which can trigger the control circuit to work is N_e, there will be

$$N_e = \begin{cases} (W_P - t_r)/\Delta T = (t_d - 2t_r)/\Delta T, t_d > 2t_r \\ 0, t_d < 2t_r \end{cases} \quad (8)$$

If a special pulse among N_e phase coincidence pulses to start the counter gate and another pulse to stop it, which is in the same position among another N_e phase coincidence as the pulse to start the counter gate, that won't generate errors. The counter gate error will be reflected as counter value error, the frequency measurement error is

$$\delta = \Delta N_x / N_x \quad (9)$$

where N_x is the counter value of f_x, and ΔN_x is the maximum error of counter value. ΔN_x is caused by Δk, which is the position difference of two pulses triggering the counter gate in their own phase coincidence pulses group.

$$\delta = \Delta k B' / N_x \quad (10)$$

In equation (10) B' is determined by the frequency relationship of f_0 and f_x. If the frequency relationship of f_0 and f_x is determined, and the counter gate τ is determined too, N_x will be determined, then the frequency measurement error only depends on Δk. The fewer N_e, the smaller Δk will be. According to the equation (8), if the time delay t_d is slightly larger than $2t_r$, the value of N_e will be very small, and Δk will be decreased, then the resolution of frequency measurement will be improved finally. When f_x is constant, selecting an appropriate f_0 will make the least quantization phase shift resolution of them a proper value, and the resolution of frequency measurement will also be improved.

III. System Design of Ultrahigh Resolution Frequency Measurement Scheme

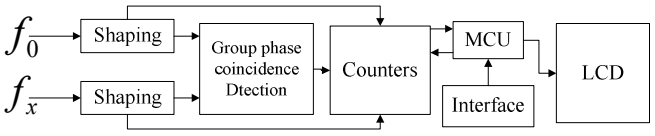

Figure 3. System Block Diagram of Ultrahigh Resolution Frequency Measurement Scheme

Fig.3 shows the block diagram of the system. The count gate is generated by the group phase coincidence detection after f_0 and f_x have been shaped, and the gate controls the operation of counter. The MCU calculates the frequency value of f_x according to the count result, and controls the LCD to display the result calculated. The man-machine interface is used to set the gate of system, frequency standard value and other parameters alike. The core of system is a high Cost-effective CPLD EPM240T100C3 of the MAXII series of ALTERA Corporation, which is used to implement the digital logic. Because of using the devices of C3 series, of which the speed level is high, and gate delay is small, the operation frequency limit of the system is very high. So the signal with the frequency as high as 350MHz can be measured. Using a high stable OCXO with the nominal frequency 10000010Hz as the internal frequency standard, f_0, there is a proper ΔT between f_0 and the usual frequency signal, such as 5MHz or 10MHz used in industry, so higher measurement resolution is achieved.

From the error analysis of frequency measurement scheme based on the group phase relationship, the key to improving measurement resolution lies in the design of group phase coincidence detection. The system uses the group phase coincidence detection circuit shown in Fig. 4

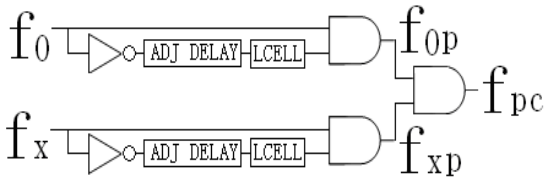

Figure 4. Group Phase Coincidence Detection Circuit

Fig.4 is added in an adjustable time delay unit compared to Fig.1. For present FPGA and CPLD, larger than 200ps time delay is easily obtained by using the special time delay unit of LCELL in EPM240T100C3, but it can not meet the high resolution of this device. So an external adjustable time

delay unit is added for the fine adjustment of the time delay besides the internal time delay unit. Fig.5 is the principle that voltage dividing delay used as fine adjustment of time delay.

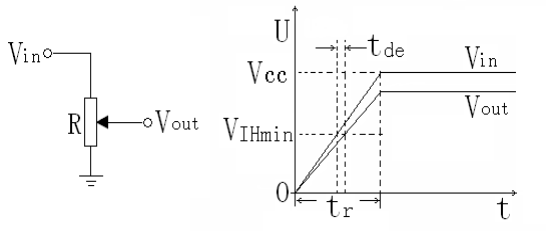

Figure 5. Principle Of Voltage Dividing Delay

t_{de} is the time delay adjusted with voltage dividing delay, by changing the resistance ratio of upper part and lower part of the potentiometer, time delay t_{de} can be adjusted easily, from Fig.5 we can know

$$0 < t_{de} < t_r/2 \quad (11)$$

Where t_r is the rising time of the input waveform, in this device, t_r is about 2ns, so t_{de} can mostly reach 1ns. From experiments, the resolution of the adjustment of time delay can reach 5ps using this method and the time delay is very stable.

The total time delay of the group phase coincidences detection circuit is

$$t_d = t_{de} + t_{di} \quad (12)$$

where t_{di} is the internal fixed time delay generated by LCELL cascade of EPM240C3, it is slightly lower than $2t_r$, then by fine adjustment of t_{de}, the total time delay t_d is slightly higher than $2t_r$, from equation (8), when t_d is slightly higher than $2t_r$, the number of effective pulse N_e and Δk will be very small, then the measurement resolution will be improvement finally.

Ⅳ EXPERIMENT RESULTS OF THE PROTOTYPE

A. Self-calibration

Use the 10MHz internal frequency standard of the synthesizer HP8662A as the frequency standard f_0 of the prototype, and use the output signal of HP8662A as measured signal. The measurement results are in Tab.1.

TABLE I. RESULTS OF SELF-CALIBRATION EXPERIMENTS

f_x（Hz）	Frequency measured（Hz）	Frequency stability σ(/s)
5 000 010	5000009.999662±1	5.1e−14
10 000 010	10000009.999966±1	2.4e−14
200 000 010	200000010.007967±1	5.3e−15
230 000 010	230000010.008142±1	7.8e−15

The frequencies measured in Tab.1 is taken down from the LCD screen directly, the data is retained to the digit which is varying. From Tab.1 we can know the self-calibration resolution is very high, it is better than $10^{-14}/\tau$.

B. Experiment of frequency measurement

In the experiment, we use the OCXO 8607 of ultrahigh stability produced by the OSA corporation , the frequency stability of which achieves $2\times10^{-13}/s$, as the frequency standard of frequency synthesizer HP8662A, and then the HP8662A synthesizes outputs a signal of 10000010Hz, which is used as f_0 in the system, and we use another OCXO 8607 and another HP8662A to produce f_x. The experimental data is shown in Tab.2.

TABLE II. RESULTS OF FREQUENCY MEASUREMENT EXPERIMENTS

f_x（Hz）	Frequency measured（Hz）	Frequency stability σ(/s)
5 000 000	5000000.2 63847±2	6.3e−13
10 000 000	10000000.51738±1	5.2e−13
12 800 000	12800000.53 795±2	3.4e−12
16 384 000	16384000.5584±1	8.2e−12

Tab.2 shows that the measurement resolution of the prototype can reach $10^{-12}/\tau$ even the correlation of the measured signal and the frequency standard is not simple. And to the two signals of simple correlation like common 5MHz and 10MHz signals, the measurement resolution can reach $10^{-13}/\tau$.

Ⅴ CONCLUSION

This paper makes a further analysis of the principle and measurement error of the frequency measurement scheme based on the group phase relationship between two signals with different frequencies, presents a method to decrease the number of group phase coincidence pulses by fine adjustment of time delay of the delay unit, improves the precision of group phase coincidence detection, thus improves frequency measurement resolution greatly, which is approximately $10^{-13}/\tau$ order of magnitude. The system can be widely used in occasions that need high resolution frequency measurement, such as the manufacture of crystal oscillator, the comparison of atom frequency standard and so on. With the improvement of the speed and resolution of electronic devices, the group phase coincidence pulses can be detected more accurately, and higher frequency measurement resolution can be achieved.

REFERENCES

[1] Wei Zhou, Systematic Research on high accuracy frequency measurements and control[D]. Japan: Shizuoka University , 2000 ,pp31~39

[2] Faxi Chen, A novel PLL based on phase comparison between two signals with different frequencies[C]. Frequency Control Symposium, 2008 IEEE International, Hawaii, America: 19-21 May 2008, Page(s):156 - 158

[3] Wei Zhou, The Frequency Measurement Technique by Broad-Band Phase Detection [J]. Chinese Journal of Scientific Instrument, 1993（4）1-6

[4] Ryszard S , Jozef K. Interpolating time counter wit h 100 ps resolution on a single FPGA device[J] . I E EE Trans . on Instrumentation and Measurement , 2000 , 49 (4) : 8792882.

[5] Altare Corporation . MAXII Device Handbook[DB/OL] http://www.altera.com.cn/literature/hb/max2 , 2005.